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	REVISION HISTORY							
CRII	PTION	DATE	APPROVED					
IL A	WITH PINOUT	6/7/2017	KMW					
OR	ORIGINS PG.2	8/21/2017	KMW					
TO BE USED FOR MANUFACTURE OR INSPECTION								

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PIN FUNCTIONS					AB	SOLUTE MAX	IMUM RATI	NGS	1		
PIN #		FUNCTION	NOTES		Parameter			Limit		Notes	
1		USB DATA-	NOTE 1.5		Vin to GND			±12V		NOTES 1,2	2
2		USB DATA +	NOTE 1.5		Logic I/O to GNI	0-0	.3V to Vin+0.	3V AND no	t to exceed +5.4	/ NOTES 2,3	}
3	Vin	POWER SLIPPLY +			GPIO1 to GND			±12V		NOTE 2	
		UART receive			DISABLE to GNE)		±12V		NOTE 2	
4	RxD	(host to CV5)	NOTE 1		GND to CHASSIS	5		±12V		NOTE 2	
		UART transmit	T transmit		Operating Tempera	ture		40°C to +8	5°C		
5	TxD	(CV5 to host)	NOTE 1	L	Mechanical Shoc	K		500g			
6	GPIO3	LOGIC LEVEL GPIO	NOTE 4	1	NOTE 1: Power supply is PROTECTED against $\pm 12V$, but will not OPERATE over that full						
		LOGIC LEVEL GPIO			range. See I	NTERFACE OP	ERATING SPE	CIFICATIO	NS table for oper	ational limits.	
7	GPIO1	(and pps input)	NOTE 3		NOTE 2: Also protecte	d against ESL) and other hi	gh-voltage	/ low-energy trar	isients.	
		SIGNAL GROUND &	JAL GROUND &			15. KXD, TXD,		DP, GPIOZ,	GPIOS		
8	GND	POWER SUPPLY RETURN									
9	GPIO2	LOGIC LEVEL GPIO	NOTE 4			INTERF	ACE OPERATI	NG SPECIF	ICATIONS		
10	LC	LOGIC LEVEL DISABLE			Paramete	er	MIN	TYP	MAX	NOTES	_
10	DISABLE	(OPEN OR LOW = ENABLE)			Power Supply Vol	tage (Vin)	+3.2V		+5.2V	Note 1	-
MOUNTING					Power Consur	nption		200mV	V		
HOLES	CHASSIS	CHASSIS GROUND	NOTE 2		DC Input Logic	_ow (Vil)			0.9V	NOTES 1,2,3	
NOTE 1: prima	ary interface com	nunications is via either uart or usb.			DC Input Logic H	ligh (Vih)	2.1V			NOTES 1,2,3	
unused interface pins may be left unconnected			DC Output Logic	Low (Vol)			0.4V	NOTES 1,2,4			
NOTE 2: for best EMC performance, tie CHASSIS (i.e. the three mounting				DC Output Log	ic High	2.6V			NOTES 1,2,4		
noies) to a local ground (e.g. pcb groundplane, altrame ground, etc.) CHASSIS and GND can be the same or different grounds, see				Disable Input T	nreshold	0.4V		1.6V	NOTES 1,5		
ABSOLUTE MAXIMUM RATINGS table for limits				NOTE 1: All voltages are referenced to the GND pin (pin 8). NOTE 2: Applies to pins: RxD, TxD, USBDM, USBDP, GPIO1, GPIO2, GPIO3. NOTE 3: Nominal input impedance at RxD pin is 10Kohm to +3V.							
NOTE 3: currently implemented as input only for Pulse Per Second (PPS) timing input. leave unconnected or wire to GND if not used.									N		
NOTE 4: future functionality; not currently implemented. these pins can be left unconnected, or wired to GND, or wired to a TTL/CMOS					Nominal inpu	t impedance a	at USBDP nin	pins is 40ki is 1Kohm ti	3 + 3V		
compatible device for possible future usage.					Nominal inpu	t impedance a	at USBDM pin	is 40Kohm	to +3V.		
comp		possible future usade.									
comp NOTE 5: CV5-1	10 does not make	use of USB connections (pins 1/2)	hese	N	NOTE 4: Applies when	sourcing/sink	king up to 6m	۹.			
comp NOTE 5: CV5- pins i	10 does not make may be left uncon	use of USB connections (pins 1/2) t nected if USB is unused.	hese		NOTE 4: Applies when NOTE 5: Nominal inpu	sourcing/sink t impedance a	ting up to 6m. at DISABLE pi	A. n is 1Mohm	to GND when DI	SABLE	
comr NOTE 5: CV5- pins	10 does not make may be left uncor	use of USB connections (pins 1/2) to nected if USB is unused.	rhese RICAL O		NOTE 4: Applies when NOTE 5: Nominal inpu voltage is be or left uncor	sourcing/sink t impedance a tween 0V and nected when	ting up to 6m, at DISABLE pi 1 +5.6V. The unused.	A. n is 1Mohm DISABLE p	to GND when DI in can be tied to	SABLE GND	
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comp NOTE 5: CV5- pins	10 does not make may be left uncor	suse of USB connections (pins 1/2) to nected if USB is unused. SHEET 5/5 ELECT PROPRIETARY NOT THE INFORMATION CONTAIN US PROPRIETARY TO LORD	RICAL O	VERVIEW	NOTE 4: Applies when NOTE 5: Nominal inpu voltage is be or left uncor PECIFIED DSES INTERSECTION	sourcing/sink t impedance a tween 0V and nected when	at DISABLE pi at DISABLE pi 1 +5.6V. The unused. COI	A. n is 1Mohm DISABLE p RPORAT ston, VT (to GND when DI in can be tied to ION 15495	SABLE GND	D
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